Methodology on Semiconductor Technology based Dual Modulus Prescaler

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*Abstract-----*CMOS refers to both a particular style of digital circuit design and the family of processes used to implement that circuitry on an integrated circuit (chips). Due to the low power dissipation by the MOS devices, the use of them is quite prominent in the VLSI. Semiconductor technology based Dual Modulus Prescaler is to be fabricated in 90 nm technology. It basically comprises of 2 blocks for controlling the pulses generated at the output i.e. 256 or 257. The synchronous divide-by-4/5 divider uses symmetric fashion D flip-flops to achieve more than 10 GHz maximum operating frequency. Also, the technology that has been used for construction of the D flip flop is of most basic components i.e. the nMOS gates and the inverters. Here, the inverters are constructed by using the NAND gates. This has simply done by shorting the two terminals of the NAND gate and making it as an inverter. The same can be done by using NOR or any other gate too. The use of this design will make the consumption of the power in microwatt as the source couple logic used in the previous design concepts has power consumption in mW [1]. This modules output is to be carried out by using the Micro wind software 3.1. The prescaler will require upto 1.2-V supply. The prescaler's estimated operating frequency is upto 17 GHz.

*Index Terms-----*Dual modulus prescaler, CMOS and low power.

I. INTRODUCTION

With the expanding need in terms of the low power consumption and increasing frequency of operation, CMOS has been the key element to fabricate the components. Also, the highest operating frequencies of prescalers implemented in GaAs and SiGe bipolar technologies have reached 27 GHz [3] and 36GHz [4]. Bipolar technologies do offer a high range of frequency of operation but at the expense of power consumption. So, to minimize the power is of prime importance. The prescaler block do consists of various submodules which comprises of nMOS and pMOS. These transistors can be effectively used so as to reduce the area as well as the power consumption. The D flip Flop internal circuit is also presented along with the waveform and the power consumption has been brought to µW. Here, we can use NOT gates and transistors to reduce the power consumption to 5.4 µW. Compared with these, the prescalers fabricated in CMOS processes usually operate at lower frequencies. The highest reported operating frequency for CMOS prescalers is 15GHz [6], [7]. The circuit has been fabricated in a 130-nm technology and consumes relatively high power (115mW).

The reason why MOS technology is preferred over BJT is as under:

Table 1: MOS and BJT comparison

Sr. no.	Parameters	BJT	MOS
1.	Thermal Runaway	Yes	No
2.	Power consumption	More	Less
3.	Input impedance	Low	High
4.	Area on chip	Less	More

Extra feedback networks were used [5] to increase the operating frequency to 14 GHz in a 0.18 µm CMOS process. A phase-shifting prescaler switches among signals with varying phases to achieve two or more divide ratios. The highest operating frequency for phase shifting prescalers [6] is 13 GHz and consumes 41 mW of power.

A dual-modulus prescaler is one of the complicated building blocks in phase lock loops. The maximum operating frequency of prescaler sets the PLL. But when the question comes of power consumption, then we have to go with the CMOS technology. The survey on prescalers has the focus on the reduction of the chip size and the power consumption. The design of low-power high-frequency divide-by N/N+ 1 dual modulus prescaler is a bit challenging. The 90 nm technology will have the pull-up and pull-down PMOS and NMOS so that the signal strength does not become weak which forms the input to the AND gate for the extra clock pulse to get added i.e. 257 pulses at the output. This paper presents a low-voltage low-power 256/257 dual-modulus prescaler. . The circuit is to be fabricated in a 90-nm CMOS process and estimated voltage will be upto 1.2-V. This forms the main voltage that is given to the circuit.

II. CIRCUIT DESIGN

A. The 1 pulse addition/ subtraction block.

The dual-modulus prescaler consists of a synchronous divide-by-4 and divide-by-5 counters and an asynchronous divide-by-64 circuit as shown in Fig. 1. The output pulses are controlled with the help of mode control (MC) which is either set to low and high to get 256 or 257 pulses respectively. The main element is the synchronous divide-by-4/5 circuit because it operates at the highest frequency as the input or the reference frequency which is given from the master oscillator. Also, we can add the reset logic so as to successfully put the entire system in the initial state. The

circuit when gets a high pulse at the output of the 7 input AND gate, the pulses that the prescalers acts is 257 pulses that is when the total number of pulses are 257, at the input, then and then the final output will be 257. The condition reverses when the number of pulses at the input are 256 i.e. here the output of the 7 input AND gate is low.
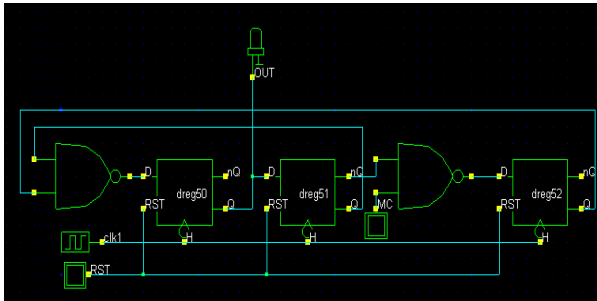

Fig. 1: The 1 pulse add/sub block in DSCH

Here, the upper section consists of the 4/5 divider network which comprises of 3 D flip flops along with 2 NAND gates. This forms the main section in the Dual Modulus Prescaler. The longest RC delay associated with the path limits the prescaler maximum operating frequency. To reduce the propagation delay, the NAND gate and flip flop are merged together. To better balance the delays, the output of first flip-flop is chosen to drive the asynchronous divider. Here, the circuit continues such that the D flip flop i.e. towards left feeds the output to the clock of the divide by two counter which is nothing but the D flip flop whose output is fed back to the input so as to operate it as a divide by two counter.
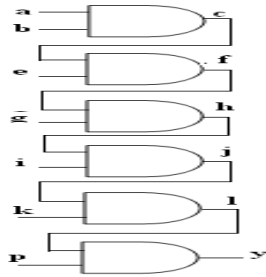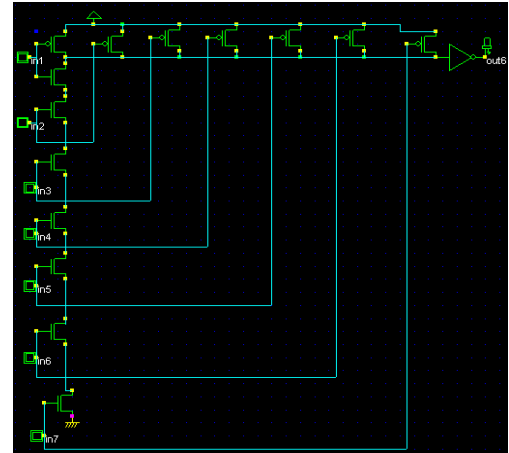

Fig. 2: A 7 input AND gate
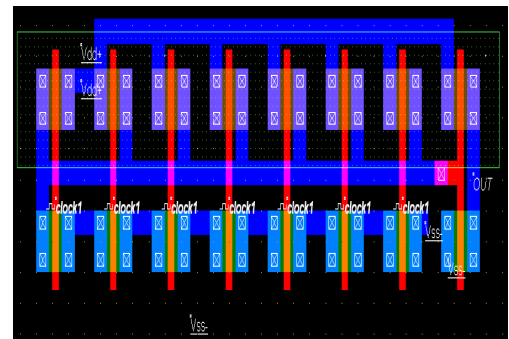

Fig. 3: 7 Input AND Gate in DSCH

Fig. 4: Layout of Seven Input AND-gate in Microwind.

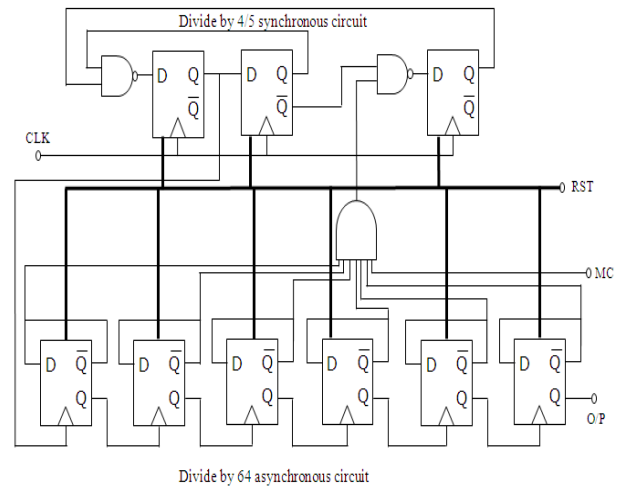The power consumption of the above circuit is: 4.9 µW and the technology used is 90 nm.

Fig. 5: A Dual Modulus Prescaler

B. Core of the System.

Due to the circuit complexity, the problem of area and capacitance effect is the major issue. So, to keep the spacing between two parallel vias is important. This spacing automatically increases the area. Also, if the number of components on chip increases, the area again increases and so the power consumption. A design of D flip flop is presented which consists of a fewer components to reduce the power consumption.
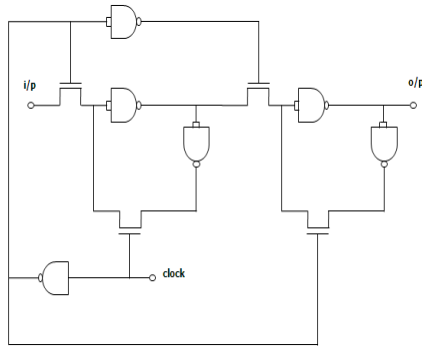

Fig. 6: A D flip-flop with NMOS and inverter

Fig. 6 shows the implementation of D flip flop used in the divide by-4/5 circuit. We have designed it using NAND, NOR or any other basic gate. But this is completely different. The circuit is like cascading of two similar blocks. Block one includes two nMOS and the first 2 inverters. The rest of the circuit is the repetition of the first part. As you can see in the schematic, the circuit involves only two basic elements i.e. the nMOS and an inverter. You can see that the clock which we are using are of two types; one is clock and the next is its complement that is clk_bar. For that we need an extra inverter.
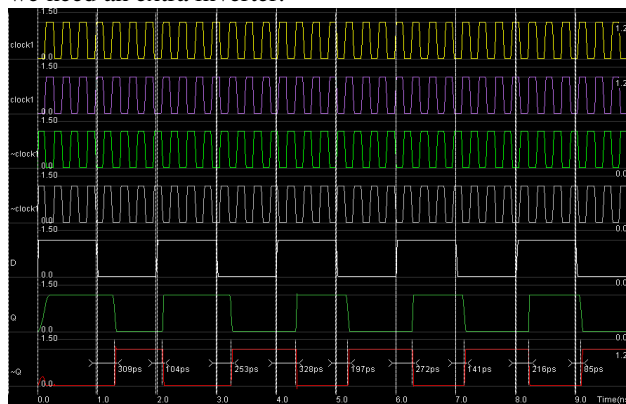

Fig. 7: Output of D flip flop

C. The Divide by 64 Unit.

It is a chain of divide by 2 asynchronous counter. As per the Sequential Logic concept, D-type flip-flop can be connected together to form a Data Latch. Another useful feature of the D-type Flip-Flop is as a binary divider, for frequency division or as a "divide-by-2" counter. Here, the inverted output terminal Q (NOT-Q) is connected directly back to the Data input terminal D giving the device "feedback".
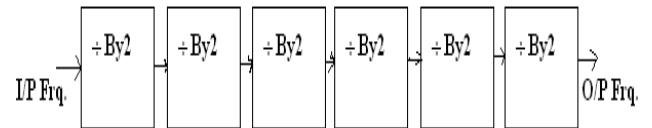

Fig. 8: Divide by 64

It can be seen from the frequency waveforms below, that by "feeding back" the output from NOT Q to the input terminal D, the output pulses at Q have a frequency that are exactly one half of the input clock frequency. In other words, the circuit produces frequency division as it now divides the input frequency by a factor of two.
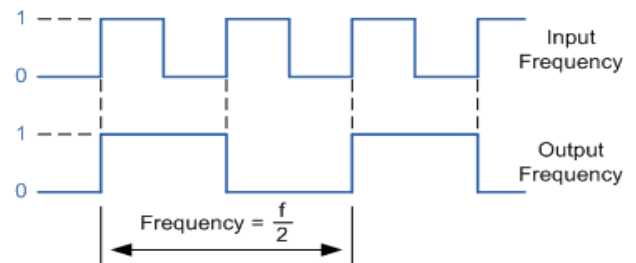

Fig. 9: Concept of divide by 2

CONCLUSION

This paper focuses on the implementation of prescaler in 90 nm technology and to bring the usage of the entire circuit in µW as the other designs so far implememted has it in mW. Also, the power reduction is the main motto as the use of prescalers is mostly in the embedded systems such as cell phones where power consumption in the main factor to be considered. These embedded systems being battery operated, they need to be continuously charged or batteries need to be replaced. The paper reflects the survey made from different IEEE papers whose titles are included in the references and the objective is to carry out the implementation of the 256/257 pulses in more effective manner. The future scope can include the use of MUX logic so that more than 2 divide ratios can be achieved. The MUX will act as the selection unit for choosing the divide ratio at the ouput.

ACKNOWLEDGMENT

REFERENCES

[1] A Low-Power 17-GHz 256/257 Dual-Modulus Prescaler Fabricated in a 130-nm CMOS Process, pp 465-468 Yanping Ding and Integrated Circuits Symposium.

[2] C.-M. Hung, B. A. Floyd, and K. K. 0, "A fully integrated 5.35-GHz CMOS VCO and a prescaler." Dig. Papers 2000 IEEE RFIC Symp, May 2000, pp. 69-72.

[3] H. Knap, M. Wurzer, T. F. Meister, .I. Bock and K. Aufinger, "36 GHz dual-modulus prescaler Kenneth K.,2005 IEEE Radio Frequency in SiGe bipolar technology." Dig. Papers 2002 IEEE RFIC Symp., June 2002, pp. 239-242

[4] S. Wada, T. Maeda, M. Tokushima, J. Yamazaki and M. lshikawa snd M. Fbjji, "A 27GHz/151mW GaAs 256/258 Dual Modulus Prescaler IC with 0.1 pm Double-Deck-Shaped (DDS) Gate E/D-HJFETs", in GAS ICSymposium Digest, pp. 125-128, 1998.

[5] M. Mizuno, H. Suzuki, M. Ogawa, K. Sato, and H. Ichikawa, "A 3-mW 1.0-GHo Silicon-ECL Dual Modulus Prescaler IC," IEEE Journal of Solid-State Circuits, vol. 27, no. 12, pp. 1794 1798, Dec. 1992.

[6] H.-D. Wohtmuth, and D. Kehrer, "A 15 GHz 256/257 dual modulus prescaler in 120 nm CMOS." European Solid- State Circuits Conference, Sep. 2003, pp. 77 - 80.

[7] H.-D. Wohlmuth, and D. Kehrer, "A 17 GHz dual- Modulus prescaler in 120 nm CMOS." Dig.Papers 2003 IEEE RFIC Symp., June 2003, pp. 479-482.

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